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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,966	08/22/2003	David J. Corisis	2269-4814.2US (01-0040.02	1076

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EXAMINER	
ZARNEKE, DAVID A	
ART UNIT	**PAPER NUMBER**
2829	

DATE MAILED: 03/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,966	CORISIS ET AL.	
	Examiner	Art Unit	
	David A. Zarneke	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/22/03;12/4/03;2/17/04;6/4/04*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 18 is rejected under 35 U.S.C. 102(b) as being clearly anticipated by Golshan et al., US Patent 5,384,488.

Golshan (figures 1 and 4) teaches a rerouting element for use with a semiconductor device, comprising:

a base substrate [38 and 40];

a plurality of conductive vias [42] positioned adjacent at least two peripheral edges of said the base substrate, each conductive via of said the plurality of conductive vias being located so as to align with a corresponding, peripherally located bond pad [16] of the semiconductor device upon assembly of-said the rerouting element with the semiconductor device;

a plurality of conductive traces [18 & 48]; and

a plurality of contact pads [26], each conductive trace of said the plurality of conductive traces extending from a corresponding conductive via toward at least one other peripheral edge [20 & 22] of said the base substrate to a corresponding contact pad of said the plurality of contact pads.

Claims 18, 21 and 22 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Akram et al., US Patent 6,072,236.

Akram (figures 6 and 7) teaches a rerouting element for use with a semiconductor device, comprising:

a base substrate [20];

a plurality of conductive vias [22] positioned adjacent at least two peripheral edges of said the base substrate, each conductive via of said the plurality of conductive vias being located so as to align with a corresponding, peripherally located bond pad [16] of the semiconductor device upon assembly of-said the rerouting element with the semiconductor device;

a plurality of conductive traces [114]; and

a plurality of contact pads [116], each conductive trace of said the plurality of conductive traces extending from a corresponding conductive via toward at least one other peripheral edge of said the base substrate to a corresponding contact pad of said the plurality of contact pads.

With respect to claim 21, Akram teaches the plurality of conductive vias are positioned adjacent to two adjacent peripheral edges of said the base substrate.

Regarding claim 22, Akram teaches each contact pad of said the plurality of contact pads is positioned adjacent to at least one of two other adjacent peripheral edges of-said the base substrate (figure 6).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Haba et al., US Patent 6,376,904, in view of Akram et al., US Patent 6,072,236.

Haba (figures 10-13) teaches semiconductor device assembly, comprising:

a first semiconductor device [1002] including a surface with a plurality of centrally located bond pads;

a rerouting element positioned over-said the first semiconductor device, said the rerouting element comprising:

a base substrate [1104];

a plurality of conductive vias [1008] located so as to align with a corresponding, centrally located bond pad of the first semiconductor device upon assembly of said the rerouting element with the first semiconductor device;

a plurality of conductive traces [1012]; and

a plurality of rerouted bond pads [1010], each conductive trace of said the plurality of conductive traces extending from a corresponding conductive via of the plurality of conductive vias toward at least one peripheral edge of said the base substrate to a corresponding rerouted bond pad of said the plurality of rerouted bond pads;

and

a second semiconductor device positioned over a portion of said the rerouting element, each of said the plurality of rerouted bond pads being exposed beyond a periphery of said the rerouting element (figure 13).

Haba fails to teach the first semiconductor device with a plurality of peripherally located bond pads and a rerouting element with vias located over the peripherally located bond pads and rerouting these bond pads to at least one other peripheral edge of the rerouting element.

Akram (figures 6, 7 & 10) teaches chips with peripherally located bond pads [16] a rerouting element for use with a semiconductor device, comprising:

a base substrate [20];

a plurality of conductive vias [22] positioned adjacent at least two peripheral edges of said the base substrate, each conductive via of said the plurality of conductive vias being located so as to align with a corresponding, peripherally located bond pad [16] of the semiconductor device upon assembly of-said the rerouting element with the semiconductor device;

a plurality of conductive traces [114]; and

a plurality of contact pads [116], each conductive trace of said the plurality of conductive traces extending from a corresponding conductive via toward at least one other peripheral edge of said the base substrate to a corresponding contact pad of said the plurality of contact pads.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the chip with peripherally located bond pads and the rerouting element of Akram in the invention of Haba because this allows the stacked package of Haba to be used with different chip types having bond pads located in different locations than the ones taught by Haba.

Regarding claim 2, Akram teaches each rerouted bond pad of said plurality of rerouted bond pads is located laterally adjacent a periphery of said the first semiconductor device (figure 6).

With respect to claim 3, Akram teaches each rerouted bond pad of said the plurality of rerouted bond pads is located adjacent a single edge of said the first semiconductor device (figure 6).

As to claim 4, Haba teaches a carrier substrate [420].

In re claim 5, Haba teaches the first semiconductor device is secured to said carrier substrate (figure 13).

Regarding claim 6, Haba teaches the carrier substrate comprises at least one of a circuit board, an interposer, another semiconductor device, and leads (5, 41+).

With respect to claim 7, Haba teaches the at least one rerouted bond pad is in communication with a corresponding contact area of the carrier substrate (figure 13).

As to claim 8, Haba teaches a discrete conductive element positioned between the at least one rerouted bond pad and said the corresponding contact area (figure 13).

In re claim 9, Haba teaches the discrete conductive element comprises at least one of a bond wire, a tape-automated bond element trace, and a lead (figure 13).

Regarding claim 10, Haba teaches another rerouting element on a bond pad-bearing surface of the second semiconductor device (figure 13).

With respect to claim 11, Haba teaches the second semiconductor device is oriented in staggered relation to-said the first semiconductor device (figure 13).

As to claim 12, while both Akram and Haba fail to teach the second semiconductor device is smaller than the first semiconductor device, the relative size of the first and second chip is an obvious matter of design choice. Design choices and

changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

In re claim 13, Haba teaches at least one additional semiconductor device positioned over-said the second semiconductor device (figure 13).

Regarding claim 14, Haba (figure 3A) teaches an encapsulant [425] protecting at least portions of said the first semiconductor device, the second semiconductor device, the discrete conductive element, and portions of the carrier substrate located laterally adjacent outer peripheries of the first and second semiconductor devices.

With respect to claims 15 and 16, while both Haba and Akram fail to teach the specific type of encapsulant, it would have been obvious to one ordinary skill in the art at the time of the invention to optimize the encapsulant to be a glob-top type encapsulant or a transfer molding compound (MPEP 2144.05).

As to claim 17, Haba teaches at least one external connective element [455] in communication with at least one bond pad of the first semiconductor device (figure 13).

Claims 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Golshan et al., US Patent 5,384,488, as applied to claim 18 above.

Regarding claim 19, though Golshan teaches the plurality of conductive vias are positioned adjacent all four peripheral edges of said the base substrate (3, 14+), it would have been obvious to one of ordinary skill in the art at the time of the invention to form the conductive vias on only 3 peripheral edges because, barring a showing of unexpected results, the placement of the conductive vias is an obvious matter of design choice. Design choices and changes of size are generally recognized as being within

the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)). The location of the vias to be redistributed is not a patentable distinction.

Claims 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Golshan et al., US Patent 5,384,488, as applied to claim 18 above, and further in view of Akram et al., US Patent 6,072,236.

With respect to claim 20, Golshan, which teaches adjacent two peripheral edges, fails to teach each contact pad of said the plurality of contact pads is positioned adjacent to another, single peripheral edge of said the base substrate.

Golshan teaches each contact pad of said the plurality of contact pads is positioned adjacent to another, single peripheral edge of said the base substrate (figure 6).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the contact pad placement of Akram in the invention of Golshan because it is a simple matter of design choice. The placement of the contact pad is obvious because its placement is determined by its final use. It would have been obvious to one of ordinary skill in the art at the time of the invention to place the contact pads on one edge as opposed to two edges because of the final design usage of the package. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

As to claim 21, Golshan, which teaches placement on all four sides (3, 14+), fails to teach the plurality of conductive vias are positioned adjacent to two adjacent peripheral edges of said the base substrate.

Akram teaches the plurality of conductive vias are positioned adjacent to two adjacent peripheral edges of said the base substrate (figure 6).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the conductive via placement of Akram in the invention of Golshan because it is a simple matter of design choice. The placement of the conductive via is obvious because its placement is determined by the chip used. It would have been obvious to one of ordinary skill in the art at the time of the invention to place the conductive via on two edges as opposed to all four edges because of the design layout of the chip. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

In re claim 22, Akram teaches each contact pad of said the plurality of contact pads is positioned adjacent to at least one of two other adjacent peripheral edges of said the base substrate (figure 6).

Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram et al., US Patent 6,072,236, as applied to claim 18 above.

Regarding claim 19, Akram, which teaches vias on only two edges, fails to teach the plurality of conductive vias are positioned adjacent three peripheral edges of said the base substrate (3, 14+).

It would have been obvious to one of ordinary skill in the art at the time of the invention to place contact pads on three edges as opposed to two edges because it is a simple matter of design choice. The placement of the contact pad is obvious because its placement is determined by its final use. It would have been obvious to one of

ordinary skill in the art at the time of the invention to place the contact pads on one edge as opposed to two edges because of the final design usage of the package. Design choices and changes of size are generally recognized as being within the level of ordinary skill in the art (MPEP 2144.04(I), (IVA) & (IVB)).

With respect to claim 20, Akram teaches each contact pad of said the plurality of contact pads is positioned adjacent to another, single peripheral edge of said the base substrate (figure 6).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David A. Zarneke whose telephone number is (571)-272-1937. The examiner can normally be reached on M-F 7:30 AM-6 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William Baumeister can be reached on (571)-272-1712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David A. Zarneke
Primary Examiner
March 14, 2005